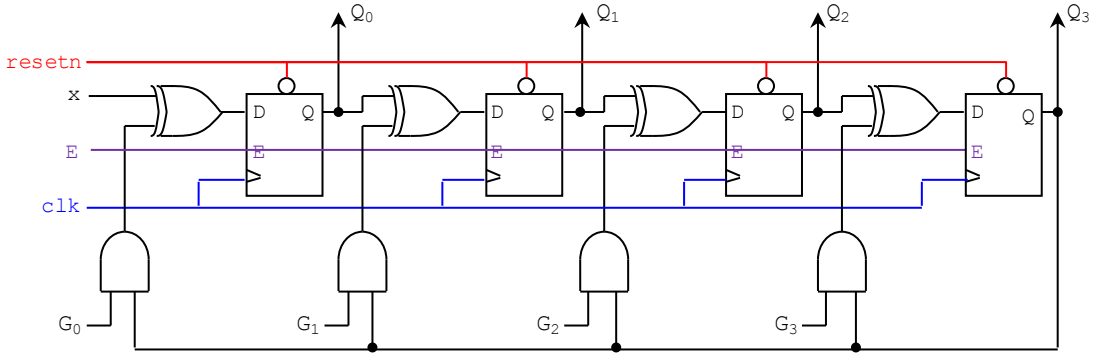
Homework 4

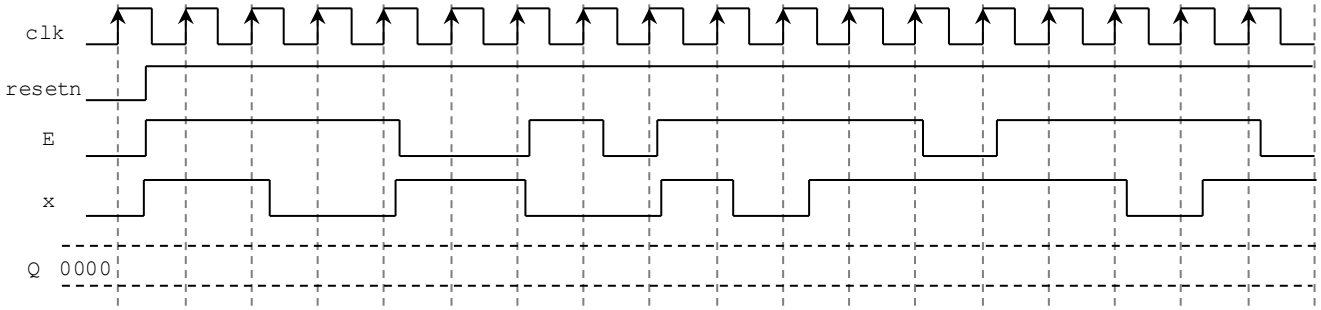
(Due date: November 17th @ 5:30 pm)

Presentation and clarity are very important! Show your procedure!

PROBLEM 1 (14 PTS)

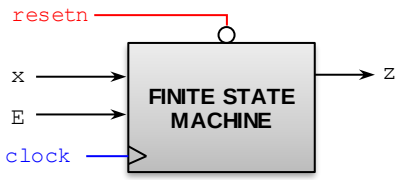
- Complete the timing diagram of the following circuit. $G = G_3G_2G_1G_0 = 1011$, $Q = Q_3Q_2Q_1Q_0$

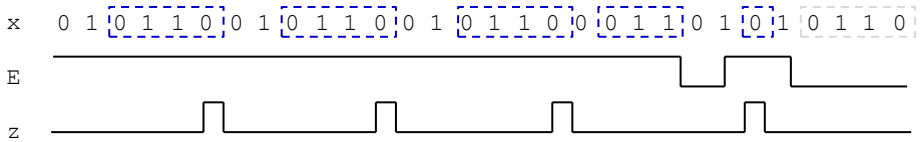




PROBLEM 2 (18 PTS)

- Sequence detector: The machine generates $z = 1$ when it detects the sequence 0110. Once the sequence is detected, the circuit looks for a new sequence.
- The signal E is an input enable: It validates the input x, i.e., if E=1, x is valid, otherwise x is not valid.

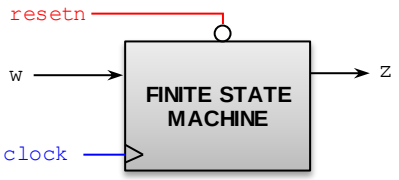




- Draw the State Diagram (any representation) of this circuits with inputs E and x and output z. (5 pts)
- Complete the State Table and the Excitation Table. (4 pts)
- Provide the excitation equations and the Boolean output equation (simplify your circuit: K-maps or Quine-McCluskey) (5 pts)
- Sketch the circuit. (3 pts)
- Which type is this FSM? (Mealy) (Moore) Why? _____

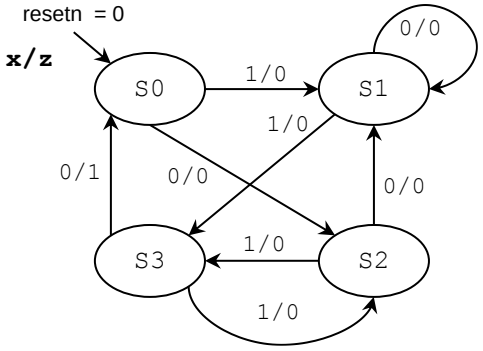
PROBLEM 3 (35 PTS)

- The following FSM has 4 states, one input w and one output z. (10 pts)
  - ✓ The excitation equations are given by:
    - $Q_1(t+1) \leftarrow Q_0(t)$
    - $Q_0(t+1) \leftarrow \overline{Q_1(t)} \oplus w$
  - ✓ The output equation is given by: $z = Q_1(t) \oplus Q_0(t) \oplus w$



  - ✓ Provide the State Diagram (any representation) and the Excitation Table (6 pts)
  - ✓ Sketch the Finite State Machine circuit. (4 pts)

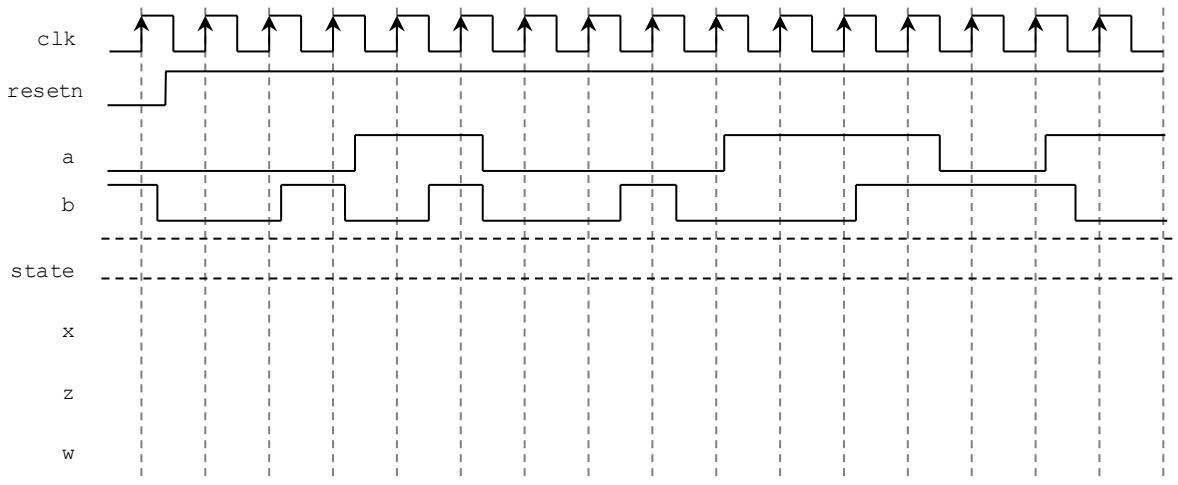
- Given the following State Machine Diagram. (10 pts)
  - ✓ Is this a Mealy or a Moore machine? Why?
  - ✓ Provide the State Table and the Excitation Table. (3 pts)
  - ✓ Get the excitation equations and the Boolean equation for z. (6 pts)
    Use S0 (Q=00), S1 (Q=01), S2 (Q=10), S3 (Q=11) to encode the states.



- Provide the state diagram (in ASM form) and complete the timing diagram of the FSM whose VHDL description is listed below. (15 pts)

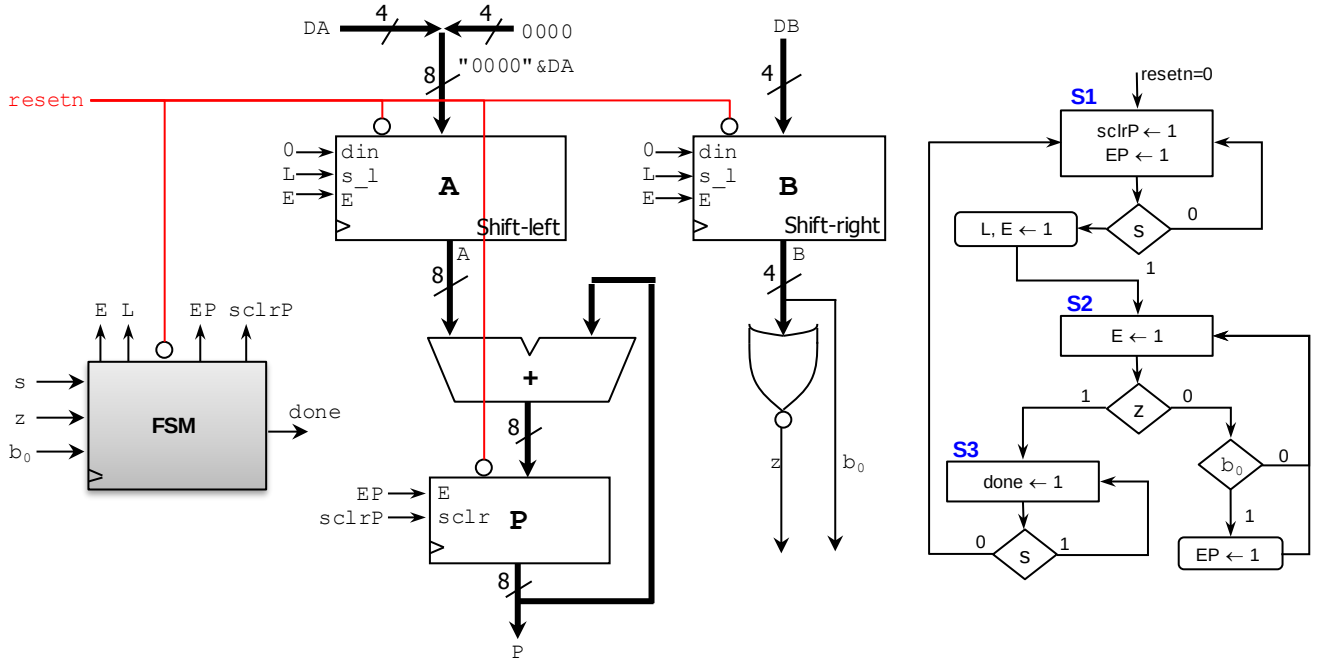
```
library ieee;
use ieee.std_logic_1164.all;

entity myfsm is
   port ( clk, resetn: in std_logic;
          a, b: in std_logic;
          x,w,z: out std_logic);
end myfsm;
```

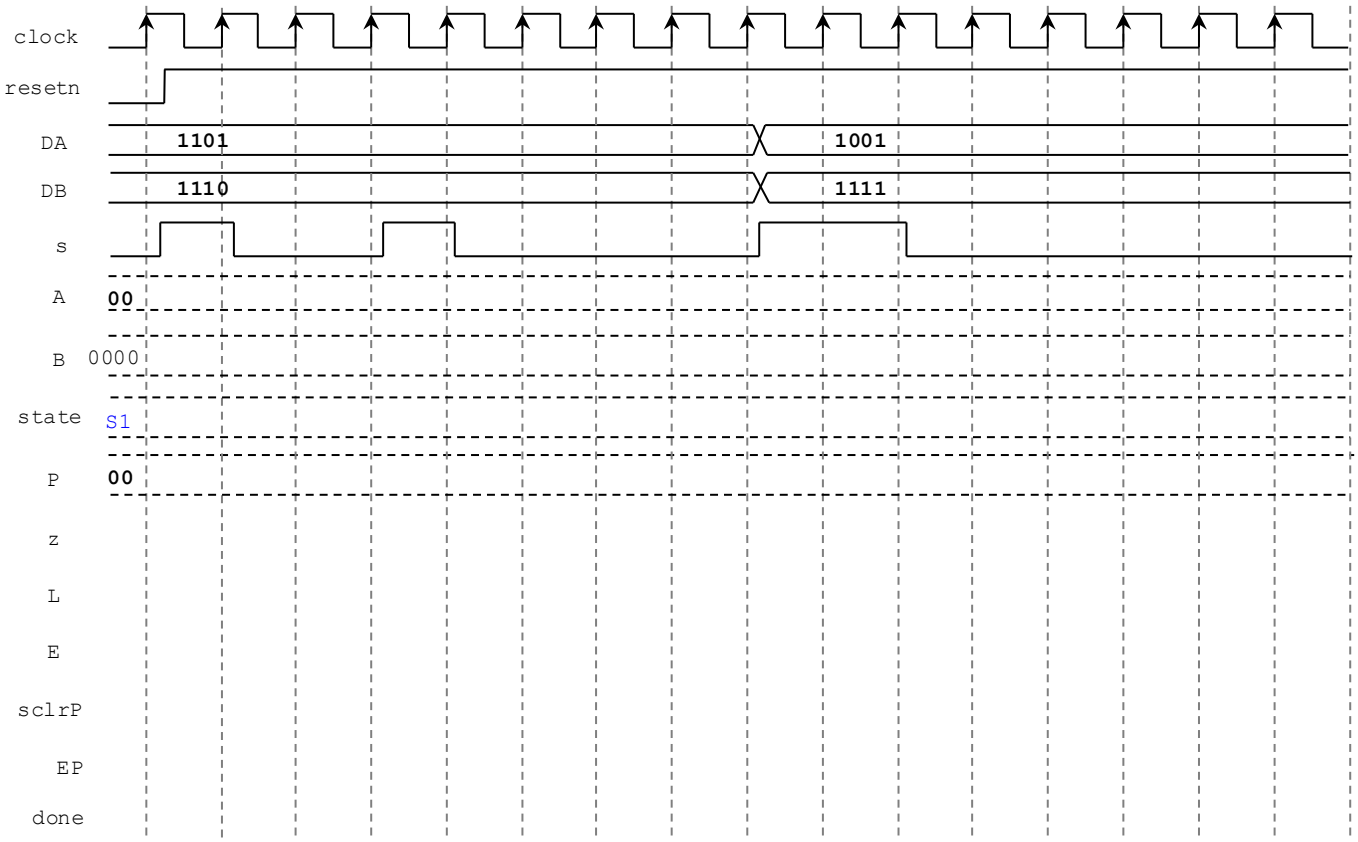
```
architecture behavioral of myfsm is
   type state is (S1, S2, S3);
   signal y: state;
begin
  Transitions: process (resetn, clk, a, b)
  begin
     if resetn = '0' then y <= S1;
     elsif (clk'event and clk = '1') then
        case y is
          when S1 =>
            if b = '1' then
              if a = '1' then y <= S3; else y <= S1; end if;
            else
              y <= S2;
            end if;

          when S2 =>
            if a = '1' then y <= S3; else y <= S2; end if;

          when S3 =>
            if a = b then y <= S3; else y <= S1; end if;
        end case;
     end if;
  end process;

  Outputs: process (y, a, b)
  begin
      x <= '0'; w <= '0'; z <= '0';
      case y is
         when S1 => if b = '1' then x <= '1'; end if;
         when S2 => w <= '1';
         when S3 => if a = b then z <= '1'; end if;
      end case;
  end process;
end behavioral;
```



PROBLEM 4 (18 PTS)

- Complete the following timing diagram (`A` and `P` are specified as hexadecimals) of the following Iterative unsigned multiplier. The circuit includes an FSM (in ASM form) and a datapath circuit.
- Refer to the Lecture Notes for mode details of the behavior of the generic components.
  - ✓ Register (for `P`): $sclr$: synchronous clear. Here, if $E = sclr = 1$, the register contents are initialized to 0.
  - ✓ Parallel access shift registers (for `A` and `B`): If $E = 1$: $s\_l = 1 \rightarrow$ Load, $s\_l = 0 \rightarrow$ Shift





PROBLEM 5 (15 PTS)

- Attach a printout of your Project Status Report (no more than 3 pages, single-spaced, 2 columns). This report should contain the current status of the project, including more details about the design and its components. You **MUST** use the provided template (`Final Project – Report Template.docx`).